Amendments to the Specification:

Please replace paragraphs 004 and 0026 with the following replacement paragraphs:

[004] Referring now to Figure 2 wherein a circuit diagram for the power-on bias circuit 2 of Figure 1 is shown. As shown in Figure 2, inverter 12 is constructed by a P-type transistor 34 and an N-type transistor 44. The substrate 42 and the source region 38 of the P-type transistor 34 are electrically connected to an input terminal 6 of the input/output terminal. The substrate 52 and the source region 50 of the N-type transistor 44 are electrically connected to ground 8. The gate 36 of the P-type transistor 34 and the gate 46 of the n-type transistor 44 are electrically connected to the output input terminal 14 of the inverter 12. The drain region 40 of the P-type transistor 34 and the drain region 48 of the N-type transistor 44 are electrically connected to the output terminal 16 of the inverter 12.

The drain region 326 of the P-type transistor 320, the drain region 364 of the N-type transistor 360, the gate 342 of the P-type transistor 340 and the gate 402 of the N-type transistor 400 are electrically connected to the output terminal 134 of the Schmitt trigger circuit 122. The source region 344 of the P-type transistor 340, the source region 324 of the P-type transistor 320 and the drain region 306 of the P-type transistor 300 are electrically connected together. The drain region 346 of the P-type transistor 340 is electrically connected to ground 126. The substrate 348 of the P-type transistor 340 is electrically connected to the input terminal 116 of the input/output terminal. The source region 406 of the N-type transistor 400, the source region 366 of the N-type transistor 360 and the drain region 384 of the N-type transistor 380 are electrically connected together, the source drain region 404 of the N-type transistor 400 is electrically connected to the input terminal 116 of the input/output terminal while the substrate 408 of the N-type transistor 400 is electrically connected to the input terminal 116 of the input/output terminal while the substrate 408 of the N-type transistor 400 is electrically connected to ground 126.